DOCUMENT SOURCE REFERENCE	
HARDWARE	Pentium PC
SOFTWARE	FrameMaker 5.5
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Digital ASIC

SAMPLE

vm

Preliminary (a)	Version S2. Created from 70-113268-02	8/16/99		
REV	**DESCRIPTION**	**DATE**	**ECO**	**SIGN**

Quantum

By: **Date** 03/01/99

ASIC Group Leader C. Wong

FMTR Block	J Appelbaum	ATA Block	W. Low
BFR Block	P. Gill	SVO	T. Luu
MTR Block	D. Do	Clock Block	D. Do
SER Block	M. Uppuluri	HNS	M. Uppuluri
UPI Block	H. Wong	ECC Block	S. Mo
Documentation	R. C. Ayeras		

DOCUMENT TITLE

Specification, Design **ASIC**

Q	DOCUMENT NUMBER	REVISION	SHEET
	R.C. Ayeras	Preliminary (a) Printed 8/22/01	1 OF 571

INTERNAL/EXTERNAL
TIMING SPECIFICATIONS
and FLOW DIAGRAMS 508

PERFORMANCE 534

TEST CASE DESCRIPTIONS 536

Q DOCUMENT NUMBER	REVISION	
R.C. Ayeras	Preliminary (a) 8/22/01	

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ASIC
VOLUME 1 - FIRMWARE

Volume 1 contains the Firmware Specification (Sections 1 through 5).

DOCUMENT NUMBER	REVISION	
R.C. Ayeras	Preliminary (a) 8/22/01	

DOCUMENT NUMBER	REVISION	
R.C. Ayeras	Preliminary (a) 8/22/01	

2.1 INITIALIZATION ROUTINES

2.1.1 Sonic Initialization

The Sonic block powers on as busy and the registers power up with all zeros. To initialize the block, the following registers must be programmed in the sequence shown below:

1) Set ATA clock to 100 Mhz in Clock block
   Set ATACLK = 8'h02
2) Set MaxLba to the capacity of the drive
   Set MAXLBA1, MAXLBA2, MAXLBA3, MAXLBA4.
3) Set MaxCHSLba to the logical CHS of the drive
   Set MAXCHSLBA1, MAXCHSLBA2, MAXCHSLBA3, MAXCHSLBA4.
4) Set the size of the write command queue
   Set WCQSIZE to the Command Queue Size.
5) Clear Interrupts (INTST)
   Set INTSTL = 8'hFF;
   Set INTSTH = 8'hFF;
   Set INTSTL2 = 8'hFF;
6) Enable Interrupt Masks (INTMSK)
   Set INTMSKL = 8'hFF;
   Set INTMSKH = 8'hFF;
   Set INTMSKL2 = 8'hFF;
7) Program Sector and Head roll over
   Set SECROLL and HEADROLL to drive configuration.
8) Program Sector Per Track and Sectors per Cylinder for CHS to LBA conversion
   Set SECPERTRK, SECPERCYLLO and SECPERCYLHI
9) Program Physical and Logical Ecc byte count
   Set LOGECCCNT and PHYECCCNT
10) Enable Commands for hardware decode (CMDENL & CMDENH)ó
    Set CMDENL = 8'hFF;ó
    Set CMDENH = 8'hFF;
11) Clear busy (set bit 4 of IFCTL 1)
12) Program Host Status register (HSTSTAT)
    Set HSTSTAT = 8'h50;

2.1.2 BFR Initialization

The BFR initialization routine follows.

```
begint
    'uwrreg (24'hff: 8783, 8'h02)
    if sdram 4mbit_10ns
        'uwwreg (24'hFF: 8780, 8'h04)              // for 4Mbit DRAM write these values
        'uwrword(24'hFF: 8062, 16'h F1C7)
    else if sdram 16mbit_10ns
        'uwrreg(24'hFF 8780, 8'h44)                // for 16Mbit DRAM put the following values
        'uwrword (24'hFF8062, 16'hF0B4)
    else if sdram 64mbit_10ns
        'uwrreg(24'hFF 87802, 8'h484)              // for 64Mbit DRAM put following values
        'uwrword (24'hFF8062, 16'hF9E7);
    endif
    uwrreg (24'hFF8061, 8'h00);
    no_op
    no_op
    uwrreg (24'FF8061, 8'h00);
end initialization routine
```

ASIC
VOLUME 2 - HARDWARE

Volume 2 contains the ASIC Hardware Specification (Sections 6 through 9).

DOCUMENT NUMBER	REVISION	
R.C. Ayeras	Preliminary (a) 8/22/01	

Q DOCUMENT NUMBER	REVISION	
R.C. Ayeras	Preliminary (a) 8/22/01	

Volume 2 Section 5
PHYSICAL DESCRIPTION

5.1 MECHANICAL SPECIFICATIONS

5.1.1 Package

176 plastic TQFP, 0.4 mm pin pitch, refer to Figure 5-1: for additional information..

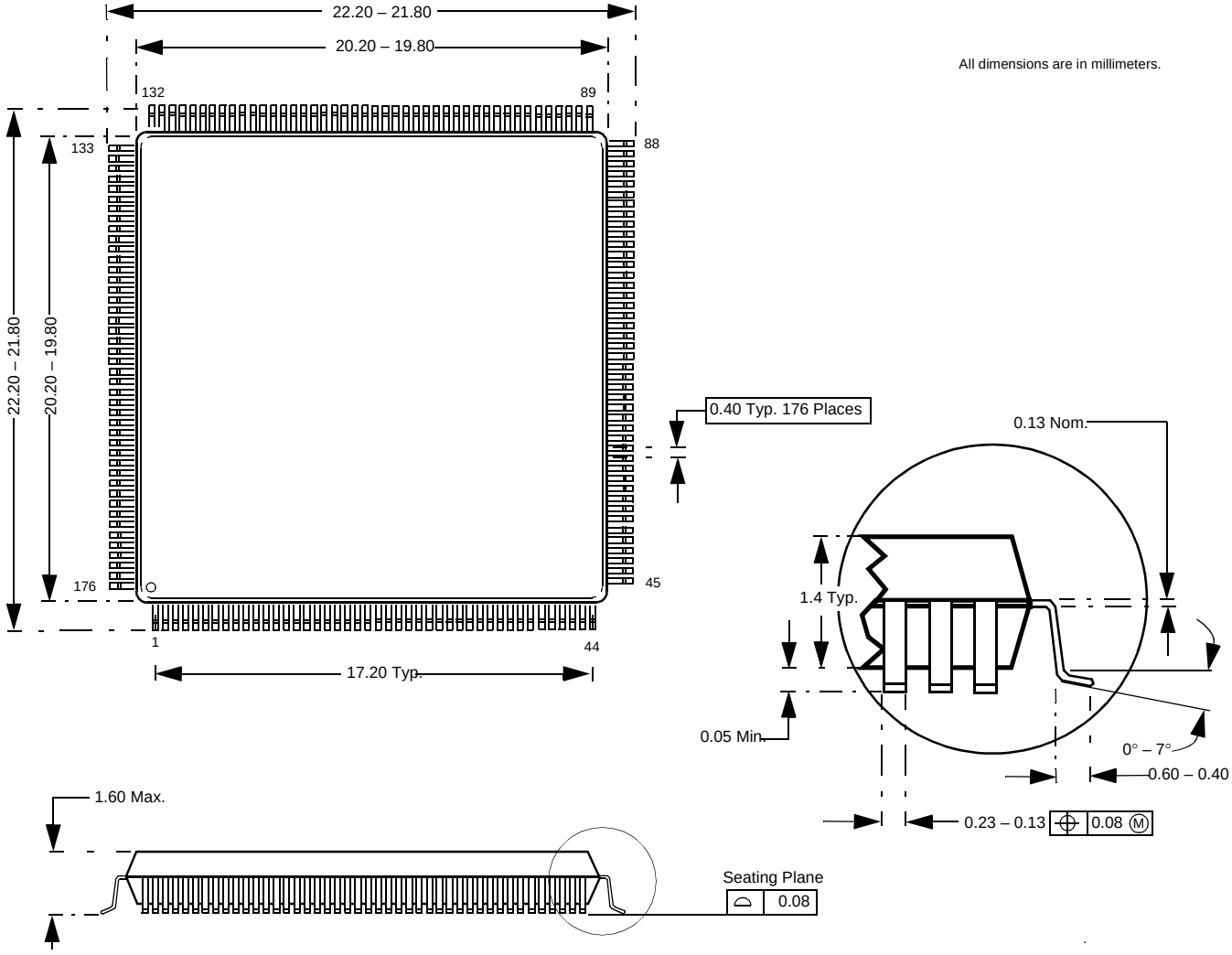


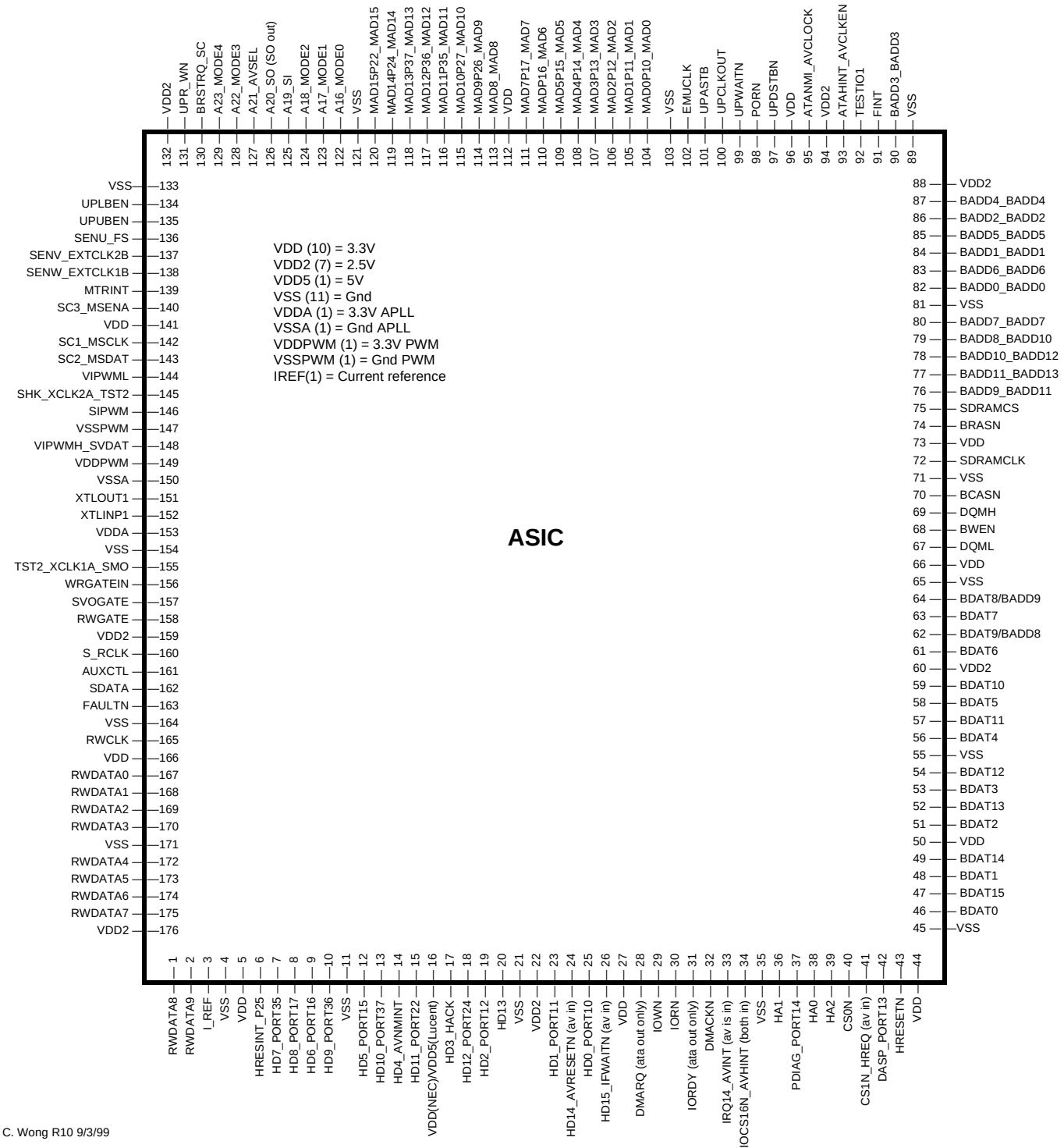
Figure 5-1: ASIC Package Specifications

5.1.2 Miscellaneous

- Low power CMOS 2.5 V/0.25 µm Standard Cell technology.
- RAM cells:
  - one (128 Words x 16 Bits 18,025 grids
  - two (64 Words x 16 Bits) 23,00 grids
  - two (64 Words x 47 bits) 61,252 grids
  - one (16 Words x 16 Bits) 6.710 grids
  - one (32 Words x 16 Bits) 8,072 grids
- NEC V850E Core 75,000 grids
- BFR Block 92,300 grids
- ECC Block 169,000 grids
- FMTR Block 59.400 grids
- µPI Block 17,800 grids
- Motor Block 20.170 grids
- Clock Block 19.700 grids
- Serial Block 2,200 grids
- Servo Block 66,500 grids
- Tmux Block 10,400 grids
- ATA Block 70,400 grids
- Cache Scan Block 61,400 grids

5.2 PINOUT

5.2.1 Pinout Drawing



C. Wong R10 9/3/99

Figure 5-2: ASIC Pinout

Pin Descriptions

Table 5-1: ASIC Pin Description

PIN NUMBER	SIGNAL NAME	DESCRIPTION
SYSTEM Total 43 Pins		
3	IREF	1. Current reference for ATA100 I/Os. 2. Requires an external resistor, 1kΩ +/- 1%, wired to ground.
152	XTLINP1	3. 40MHz resonator input 4. APLL test mode: REFCLK
151	XTLOUT1	40MHz resonator output
92	TESTIO1	1. Core test mode: Test bidi signal #29. 2. Other modes: TRIGGER IN or multiplex UDL output signals. POR default to output mode. 3. APLL test mode: VCO
155	TST2_XCLK1A_SMODE	1. ATA or A/V normal mode: TRIGGER IN or multiplex UDL output signals. 2. Core test mode: Test bidi signal #19. 3. Other modes: EXTCLK1A, or TRIGGER IN or multiplex UDL output signals. POR default to input mode. 4. APLL test mode: VCOP
16	VDD5 (1)	5v supply for the ATA interface signals.
5, 27, 44, 50, 66, 73, 96, 112, 141, 166	VDD (10)	3.3v supply pins. Pins 29 and 44 are dedicated for the UDMA IO ring.
22, 60, 88, 94, 132, 159, 176	VDD2 (7)	2.5v supply for the internal UDL and the processor core.
4, 11, 35, 45, 55, 65, 71, 81, 89, 103, 121, 133, 153, 164, 171	VSS (16)	Digital ground. Pins 12, 23, and 35 are dedicated to the UDMA IO ring.
154	VDDA	Frequency synthersizer isolated supply pin: 1. For ASIC, it is 3.3v; Also, the resonator IO shares this supply. 2. For ASIC, it is 2.5v.
150	VSSA	Frequency synthersizer isolated ground pin: 1. For ASIC, the resonator IO shares this ground pin.
149	VDDPWM	Motor PWM output signal isolated 3.3v supply.
147	VSSPWM	Motor PWM output signal isolated ground pin.
UPI I/F Total 39 pins		
104	MAD0P10_MAD0	1. ATA normal mode: Port 1, bit 0 2. ATA emulation mode: multiplexed data and address bit 0 3. A/V normal or emulation mode: multiplexed data and address bit 0 4. Core test mode: Test bidi signal #0
105	MAD1P11_MAD1	1. ATA normal mode: Port 1, bit 1 2. ATA emulation mode: multiplexed data and address bit 1 3. A/V normal or emulation mode: multiplexed data and address bit 1 4. Core test mode: Test bidi signal #1
106	MAD2P12_MAD2	1. ATA normal mode: Port 1, bit 2 2. ATA emulation mode: multiplexed data and address bit 2 3. A/V normal or emulation mode: multiplexed data and address bit 2 4. Core test mode: Test bidi signal #2
107	MAD3P13_MAD3	1. ATA normal mode: Port 1, bit 3 2. ATA emulation mode: multiplexed data and address bit 3 3. A/V normal or emulation mode: multiplexed data and address bit 3 4. Core test mode: Test bidi signal #3
108	MAD4P14_MAD4	1. ATA normal mode: Port 1, bit 4 2. ATA emulation mode: multiplexed data and address bit 4 3. A/V normal or emulation mode: multiplexed data and address bit 4 4. Core test mode: Test bidi signal #4
109	MAD5P15_MAD5	1. ATA normal mode: Port 1, bit 5 2. ATA emulation mode: multiplexed data and address bit 5 3. A/V normal or emulation mode: multiplexed data and address bit 5 4. Core test mode: Test bidi signal #5
110	MAD6P16_MAD6	1. ATA normal mode: Port 1, bit 6 2. ATA emulation mode: multiplexed data and address bit 6 3. A/V normal or emulation mode: multiplexed data and address bit 6 4. Core test mode: Test bidi signal #6
111	MAD7P17_MAD7	1. ATA normal mode: Port 1, bit 7 2. ATA emulation mode: multiplexed data and address bit 7 3. A/V normal or emulation mode: multiplexed data and address bit 7 4. Core test mode: Test bidi signal #7

Table 5-1: ASIC Pin Description (Continued)

PIN NUMBER	SIGNAL NAME	DESCRIPTION
113	MAD8_MAD8	1. ATA normal mode: **Not used** 2. ATA emulation mode: multiplexed data and address bit 8 3. A/V normal or emulation mode: multiplexed data and address bit 8 4. Core test mode: Test bidi signal #8
114	MAD9P26_MAD9	1. ATA normal mode: Port 2, bit 6 2. ATA emulation mode: multiplexed data and address bit 9 3. A/V normal or emulation mode: multiplexed data and address bit 9 4. Core test mode: Test bidi signal #9
115	MAD10P27_MAD10	1. ATA normal mode: Port 2, bit 7 2. ATA emulation mode: multiplexed data and address bit 10 3. A/V normal or emulation mode: multiplexed data and address bit 10 4. Core test mode: Test bidi signal #10
116	MAD11P35_MAD11	1. ATA normal mode: Port 3, bit 5 2. ATA emulation mode: multiplexed data and address bit 11 3. A/V normal or emulation mode: multiplexed data and address bit 11 4. Core test mode: Test bidi signal #11
117	MAD12P36_MAD12	1. ATA normal mode: Port 3, bit 6 2. ATA emulation mode: multiplexed data and address bit 12 3. A/V normal or emulation mode: multiplexed data and address bit 12 4. Core test mode: Test bidi signal #12
118	MAD13P37_MAD13	1. ATA normal mode: Port 3, bit 7 2. ATA emulation mode: multiplexed data and address bit 13 3. A/V normal or emulation mode: multiplexed data and address bit 13 4. Core test mode: Test bidi signal #13
119	MAD14P24_MAD14	1. ATA normal mode: Port 2, bit 4 2. ATA emulation mode: multiplexed data and address bit 14 3. A/V normal or emulation mode: multiplexed data and address bit 14 4. Core test mode: Test bidi signal #14
120	MAD15P22_MAD15	1. ATA normal mode: Port 2, bit 2 2. ATA emulation mode: multiplexed data and address bit 15 3. A/V normal or emulation mode: multiplexed data and address bit 15 4. Core test mode: Test bidi signal #15
122	A16_MODE0	1. ATA or A/V emulation mode: address bit 16 2. During POR, latched in as MODE bit 0 3. Core test mode: Test input #33 4. APLL test mode: M[0]
123	A17_MODE1	1. ATA or A/V emulation mode: address bit 17 2. During POR, latched in as MODE bit 1 3. Core test mode: Test input #34 4. APLL test mode: M[1]
124	A18_MODE2	1. ATA or A/V emulation mode: address bit 18 2. During POR, latched in as MODE bit 2 3. Core test mode: Test input #32 4. APLL test mode: M[2]
125	A19_SI	1. ATA or A/V emulation mode: address bit 19 2. ATA or A/V normal mode: Serial input for external FLASH upload
126	A20_SO	1. ATA or A/V emulation mode: address bit 20 2. ATA or A/V normal mode: Serial output for external FLASH download 3. APLL test mode: FRANGE
127	A21_AVSEL	1. ATA or A/V emulation mode: address bit 21 2. A/V normal mode: A/V select to ASIC 2 (output) 3. Core test mode: Test bidi signal #24 4. APLL test mode: M[3]
128	A22_MODE3	1. ATA or A/V emulation mode: address bit 22 2. During POR, latched in as MODE bit 3 3. Core test mode: Test input #37 4. APLL test mode: M[4]
129	A23_MODE4	1. ATA or A/V emulation mode: address bit 23 2. During POR, latched in as MODE bit 3 3. Core test mode: Test input #38 4. APLL test mode: N[0]
130	BRSTRQ_SC	1. ATA or A/V emulation mode: Burst transfer request (input) 2. ATA or A/V normal mode: Serial clock for external FLASH (output)
131	UPR_WN	1. ATA or A/V emulation mode: IO R/W (input) 2. A/V normal mode: IO R/W (output from core to ASIC 2) 3. Core test mode: Test bidi signal #25
134	UPLBEN	1. ATA or A/V emulation mode: IO R/W low byte enable (input) 2. A/V normal mode: IO R/W low byte enable (output from core to ASIC 2) 3. Core test mode: Test bidi signal #26

Table 5-1: ASIC Pin Description (Continued)

PIN NUMBER	SIGNAL NAME	DESCRIPTION
135	UPUBEN	1. ATA or A/V emulation mode: IO R/W high byte enable (input) 2. A/V normal mode: IO R/W high byte enable (output from core to ASIC 2) 3. Core test mode: Test bidi signal #27
95	ATANMINT_AVCLOCK	1. ATA emulation mode: Servo (NMI) interrupt (output) 2. Core test mode: Test bidi signal #28 3. AV normal and emulation mode: AV Clock
91	FINT	1. ATA or A/V emulation mode: Formatter interrupt (output) 2. ATA or A/V normal mode: SpareInt (input) 3. Core test mode: Test output #32 4. APLL test mode: N[2]
5	HRESINT_P25	1. ATA or A/V emulation mode: Host reset interrupt (output) 2. ATA normal mode: PORT 2, bit 5 (IDE_CABLE_SELECT)
93	ATAHINT_AVCLKEN	1. ATA emulation mode: Host interrupt (output) 2. AV normal and emulation mode: AV clock enable 3. Core test mode: Test bidi signal #20 4. APLL test mode: PWRDN
139	MTRINT	1. ATA or A/V emulation mode: Mighty motor interrupt (output) 2. ATA or A/V emulation mode: Redwood motor interrupt (input) 3. Core test mode: Test bidi signal #21 4. APLL test mode: N[1]
97	UPDSTBN	1. ATA or A/V emulation mode: IO R/W data Strobe (input) 2. A/V normal mode: IO R/W data strobe (output from core to ASIC 2) 3. Core test mode: Test bidi signal #22
98	PORN	1. All modes: power on reset
99	UPWAITN	1. ATA or A/V emulation mode: processor wait (output) 2. Core test mode: Test input #35
100	UPCLKOUT	1. All modes: processor clock for burst mode (3.3v failsafe)
101	UPASTB	1. ATA or A/V emulation mode: IO R/W address Strobe (input) 2. A/V normal mode: IO R/W address strobe (output from core to ASIC 2) 3. Core test mode: Test bidi signal #23
102	EMULCLK	1. All modes: Emulation clock
SDRAM I/F (Buffer) Total 37 pins		
77(MSB), 78, 76, 79, 80, 83, 85, 87, 90, 86, 84, 82(LSB)	BADD[11:0]	1. All modes: Buffer address [11:0] for 4 Mbit SDRAM, badd[7:0] 2. For 16Mb SDRAM: BADD[9:8] mapped to SDRAM pin ADD{11:10], BADD[11:10] mapped to SDRAM pin ADD[9:8], BADD[7:0] mapped to ADD[7:0]. 3. For 64 Mbit SDRAM : BADD[11:8] mapped to BADD[13:10]
62	BDAT9_BADD8	1. All modes: Buffer data bit 9 2. For 64 Nbit SDRAM : shared with BADD[8]
64	BDAT8_BADD9	1. All modes: Buffer data bit 8 2. For 64 Mbit SDRAM : shared with BADD[9]
47(MSB), 49, 52, 54, 57, 59(LSB)	BDAT[15:10]]	1. All modes: Buffer data [15:10].
63(MSB), 61, 58, 56, 53, 51, 48, 46(LSB)	BDAT[7:0]	1. All modes: Buffer data [7:0]
68	BWEN	1. All modes: Buffer write enable
69	DQMH	1. All modes: Buffer high byte enable
67	DQML	1. All modes: Buffer low byte enable
70	BCASN	1. All modes: Buffer column address strobe
74	BRASN	1. All modes: Buffer row address strobe
72	SDRAMCLK	1. All modes: Buffer clock
75	SDRAMCS	1. All modes: Buffer chip select
Motor I/F Total 10 pins		
142	SC1_MSCLK	1. Mighty : Spindle phase 1 2. Redwood : Serial port clock 3. Core test mode: Test output #33
143	SC2_MSDAT	1. Mighty : Spindle phase 2 2. Redwood : Serial port data 3. Core test mode: Test bidi signal #16
140	SC3_MSENA	1. Mighty : Spindle phase 3 2. Redwood : Serial port enable 3. Core test mode: Test bidi signal #17 4. APLL test mode: RESET

Table 5-1: ASIC Pin Description (Continued)

PIN NUMBER	SIGNAL NAME	DESCRIPTION
136	SENU_FS	1. Mighty : Sense phase U 2. Redwood : Failsafe (same as UPF) 3. Core test mode: Test bidi signal #31 4. APLL test mode: BYPASS
137	SENV_EXTCLK2B	1. Mighty : Sense phase V 2. Core test mode: Test bidi signal #30 3. APLL test mode: P[1]
138	SENW_EXTCLK1B	1. Mighty : Sense phase W 2. Core test mode: Test input #36 3. APLL test mode: P[0]
148	VIPWMH_SVDAT	1. Mighty : PWM (MSB) to control voice coil current 2. Redwood : PWM Serial port data
144	VIPWML	1. Mighty : PWM (LSB) to control voice coil current
146	SIPWM	1. Mighty : PWM to control motor current
145	SHOCK_XCLK2A_TST 2	1. Shock Sensor detection 2. EXTCLK2A 3. In Mighty mode: TESTIO2 4. Core test mode: Test bidi signal 18 5. PC debug mode: PC(18)
ATA Interface Total 31 pins		
25	HD0_PORT10	1. Normal ATA mode: HD0 2. Normal A/V mode: Port 1, bit 0 3. Program Count Debug mode: PC[1]
22	HD1_PORT11	1. Normal ATA mode: HD1 2. Normal A/V mode: Port 1, bit 1 3. Program Count Debug mode: PC[2]
20	HD2_PORT12	1. Normal ATA mode: HD2 2. Normal A/V mode: Port 1, bit 2 3. Program Count Debug mode: PC[3]
17	HD3_HACK	1. Normal ATA mode: HD3 2. Normal A/V mode: Host ACK 3. Program Count Debug mode: PC[4]
15	HD4_AVNMINT	1. Normal ATA mode: HD4 2. AV emulation mode: NMINT 3. Program Count Debug mode: PC[5]
11	HD5_PORT15	1. Normal ATA mode: HD5 2. Normal A/V mode: Port 1, bit 5 3. Program Count Debug mode: PC[6]
9	HD6_PORT16	1. Normal ATA mode: HD6 2. Normal A/V mode: Port 1, bit 6 3. Program Count Debug mode: PC[7]
7	HD7_PORT35	1. Normal ATA mode: HD7 2. Normal A/V mode: Port 3, bit 5 3. Program Count Debug mode: PC[8]
8	HD8_PORT17	1. Normal ATA mode: HD8 2. Normal A/V mode: Port 1, bit 7 3. Program Count Debug mode: PC[9]
10	HD9_PORT36	1. Normal ATA mode: HD9 2. Normal A/V mode: Port 3, bit 6 3. Program Count Debug mode: PC[10]
13	HD10_PORT37	1. Normal ATA mode: HD10 2. Normal A/V mode: Port 3, bit 7 3. Program Count Debug mode: PC[11]
16	HD11_PORT22	1. Normal ATA mode: HD11 2. Normal A/V mode: Port 2, bit 2 3. Program Count Debug mode: PC[12]
19	HD12_PORT24	1. Normal ATA mode: HD12 2. Normal A/V mode: Port 2, bit 4 3. Program Count Debug mode: PC[13]
21	HD13	1. Normal ATA mode: HD13 2. Normal A/V mode: Port 2, bit 5 3. Program Count Debug mode: PC[14]
24	HD14_AVRESETN	1. Normal ATA mode: HD14 2. All AV mode: AV reset from ASIC 2 3. Program Count Debug mode: PC[15]

Table 5-1: ASIC Pin Description (Continued)

PIN NUMBER	SIGNAL NAME	DESCRIPTION
26	HD15_IFWAITN	1. Normal ATA mode: HD15 2. ALL AV modes: Interface waitn 3. Program Count Debug mode: PC[16]
6	HRESETN	1. All ATA mode: Host Reset_
28	IOWN	1. All ATA mode: IO Write_
27	DMARQ	1. All ATA mode: DMA Request
30	IORN	1. All ATA mode: IO Read_
31	IORDY	1. All ATA mode: IO Ready
32	DMACKN	1. All ATA mode: DMA ACK_
33	IRQ14_AVINT	1. All ATA mode: IRQ14 2. All A/V mode: A/V Host Interrupt In
34	IOCS16N_AVHINT	1. All ATA mode: IOCS16_ 2. AV emulation mode: AV host Interrupt out
36	HA1	1. All ATA mode: Host Address 1
37	PDIAG_PORT14	1. All ATA mode: PDIAG_ 2. Normal A/V mode: Port 1, Bit 4
38	HA0	1. All ATA mode: Host Address 0
43	DASP_PORT13	1. All ATA mode: DASP 2. Normal A/V mode: Port 1, bit 3 3. Program Count Debug mode: PC[17]
40	HA2	1. All ATA mode: Host Address 2
42	CS1N_HREQ	1. All ATA mode: Chip Select 1_ 2. All A/V mode: Host Request
41	CS0N	1. Normal ATA mode: Chip Select 0_
R/W I/F (FMTR) Total 18 pins		
3(MSB), 2, 175, 174, 173, 172, 170, 169, 168, 167(LSB)	RWDAT[9:0]	1. All Modes: Channel data during Read, Write, and Servo operation
163	FAULTN	1. All Modes: Read channel or Preamp fault_
160	S_RCLK	1. All Modes: Channel Serial port clock & REFCLK
162	SDATA	1. All Modes: Channel Serial port data
161	AUXCTL	1. All Modes: Extended control
156	WRGATEIN	1. All Modes: Enables write data drives & preamp wrgout via quiet buffer on channel
158	RWGATE	1. All Modes: Functions as “read gate” or “write gate”, as per state of WRGATEIN
157	SVOGATE	1. All Modes: Enable servo mode operation
165	RWCLK	1. All Modes: RW clock

5.3 ASIC MODES OF OPERATION

The ASIC family has twenty-six modes of operation which are determined by the states of the five mode pins upon the rising edge of reset: PORN, 121.

The mode pins are A23, MODE4, A22_MODE4, A22_MODE3, A18_MODE2, A17_MODE1, A16_MODE0, and chip pins 155, 153, 149, 148, 146. All mode pins except A16_MODE0 have internal pull-downs; A16_MODE0 has an internal pull-up. All modes are assigned with a mode number Mxx, where xx is the decimal value from the mode pins upon POR. M0 and M1 are reserved to the ATA_Standalone and ATA_Emulation modes, respectively, so that they are compatible with Tristar.

Following is a brief description of the twenty-six modes, including debug modes.

Note: The ATA drive heads must use M0 and M1 (M10 and M11 for the AV drive team) for drive bring-up and testing. M4 for the ATA and M14 for the AV are the emergency modes which allow the core program counter value to be observed at the chip IO.

M0:ATA_Standalone

- Normal core run mode.
- External FLASH code downloaded into internal SRAM after POR (E/P builds).
- 16 programmable IO ports available on the MAD bus and “HRESINT”.
- APLLs have been checked out: They are functioning.
- Core powered up with the OSC 40 MHz: FW can switch the core clock to 33MHz, 50MHJz, or 66MHz.
- Normally, external clocks are not required: SHOCK, TESTIO2, SENV, and SENW are used. If either or both EXTCLK2 or EXTCLK1 is required, they can be received through pins SHOCK and TESTIO2, respectively.
- There must be an internal Shock Enable register bit (POR default is *disabled*). It must be set to *enabled* when SHOCK is used normally.
- Functional HW blocks provide options to select the OSC, APLL outputs, or APLL output derivatives.

M1: ATA_Emulation

- Normal emulation debug/run mode: Test Vector generation mode.
- 40 MHz OSC clock to core during POR; then use STOPB to step the core.
- 16 Programmable IO ports available from the emulator.
- If APLLs are working (normal emulation mode):
  - 13.3MHz EMULCLK (66MHz µP clock) is the POR default.FW can switch to other EMULCLK frequencies (6.6MHz, 8MHz, 10MHz).
  - External clocks are not required. SHOCK, TESTIO2, SENV, and SENW are used normally.
  - Function HW blocks provide options to select the OSC, APLL outputs, or APLL output derivatives.
- If the APLLs or the OSC are not working:
  - If NO EMULCLK, then use an external emulation clock.
  - To determine which clock is non-functional, bring out the OSC clock (POR) default) and APLL outputs to TESTIO1 one at a time.
  - Use SHOCK as EXTCLK2 to bring in 66.6MHz, and use TESTIO2 as EXTCLK1 to provide 100MHz.
  - Functional HW blocks provide the ability to select a clock that is available.
- With EXTCLK1 and EXTCLK2 brought in from TESTIO2 and SHOCK, respectively, this mode can be used to generate test vectors for all blocks except for theservo blocks and the tmux blocks. EXTCLK1 and EXTCLK2 can also be used to generate IDDQ test vectors.

M2: ATA_Standalone_Debug

- Core debug mode for checking the core/UDL interface. Similar to M0 (ATA_Standalone), with the following modifications:
  - The Core receives clock from EXTCLK2 through the SHOCK pin, instead of APLL.
  - Internal Shock Enable bit remains disabled.

M3: ATA_Emulation_Test

- Similar to M1 (ATA_Emulation) except for the following:
  - EXTCLK1 and EXTCLK2 are brought in from SENW and SENV, respectively. This mode is used to generate test vectors for the servo block and the tmux blocks, respectively. This can also be used to generate IDDQ test vectors.

M4: ATA_PC_Debug

- Similar to M0 (ATA_Standalone) except with the following:
  - ATA cable is disconnected.
  - 16 programmable IO ports are available on the MAD bus and the HRESING pin.
  - Core Program Count [18:1] are visible on ATA HD, IORN, and DASP lines.

M5: ATA_CORE_IF_TEST

- CORE/UDL Test Vector generation mode.

M6: ATA_Emulation_33

- Similar to M1 (ATA_Emulation) except that EMULCLK is set to 6.6MHz (33MHz µP clock) at POR. It can be switched to other frequencies by FW.

M7: ATA_Emulation_50

- Similar to M1 (ATA_Emulation), except that EMULCLK is set to 10MHz (50MHz mP clock) and POR. Ican be switched to other frequencies, 6.6MHz, 8MHz, or 13.3MHz, by FW.

M8: ATA_Emulation_40

- Similar to M1 (ATA_Emulation), except that EMULCLK is set to 8MHz (40MHz µP clock) at POR. It can be switched to other frequencies by FW: 6.6MHz, 10MHz, 13.3MHz.

M9: ATA_Standalone_Profile: New for V2

- Except Port2.5 (CABLE_SELECT_IDE), all programmable IO ports defined in normal ATA standalone modes (M0, M2, M4, and M5), are NOT available.
- Pins 120-113 and 111-104 are re-defined as the normal bi-directional uP MAD bus.
- All five processor control signals are driven by the Core and available on the pins UPR_WN, UPDSTBN, UPASTB, UPLBEN, and UPUBEN.
- Pin 127 (A21_AVSEL) is asserted when address between 00FF:8400h to 00FF:84FFh is decoded, indicating this is in the FW profiling arrange.

M10: AV_Standalone:

- Similar to M0 (ATA_Standalone) except with the following modifications:
- ATA interface control signal pins are re-defined to interface with ASIC 2
- UP interface pins are needed for the core to talk to ASIC 2
- Programmable I/O ports are available on the ATA interface data pins
- AV FW_Profiling functional mode

M11: AV_Emulation:

- Similar to M1 (ATA_Emulation) except with the following modifications:
- ATA control signal pins are re-defined to interface with ASIC 2

M12: AV_Standalone_Debug:

- Similar to M2 **(**ATA_Standalone_Debug) except with the following modifications:
- ATA interface control signal pins are re-defined to interface with ASIC 2
- UP interface pins are needed for the core to talk to ASIC 2
- Programmable I/O ports are available on the ATA interface data pins

M13: AV_Emulation_Test :

- Similar to M3 (ATA_Emulation_Test) except with the following modification :
- ATA control signal pins are re-defined to interface with ASIC 2

M14: AV_PC_Debug :

- Similar to M4 (ATA_PC_Debug) except with the following modifications :
- Programmable I/O ports are NOT available
- Core Program Count [18:1] are visible on ATA HD, IORN, and DASP lines

M15: AV_CORE_IF_TEST :

- CORE/UDL Test Vector generation mode
- AV FW_Profiling Test Vector generation mode

M16: AV_Emulation_33 :

- Similar to M11 (AV_Emulation) except that the “EMULCLK” is set to 6.6MHz (33MHz uP clock) at POR, and it can be switched to other frequencies by FW.

M17: AV_Emulation_50:

- Similar to M11 (AV_Emulation) except that “EMULCLK” is set to 10MHz (50MHz uP clock) at POR, and it can be switched to other frequencies (6.6, 8, or 13.3MHz) by FW.

M18: AV_Emulation_40:

- Similar to M11 (AV_Emulation) except that “EMULCLK” is set to 8MHz **(**40MHz uP clock**)** at POR, and it can be switched to other frequencies (6.6, 10, or 13.3MHz) by FW.

M19: ATA_CORE_IF_PROFILE_TEST: New for V2

- For test vector generation only (M9 is the functional mode)
- Core boot up from external SDRAM similar to M5, ATA_CORE_IF_TEST
- MAD bus, uP control signals, and A21_AVSEL are same as defined in M9.

M20: ATA/AV CORE_TEST

- Reserved for vendor Core test.

M21: ATA/AV CORE_BIST

- Reserved for Lucent Core memory test.

M22: ATA/AV DC_TEST

- Reserved for NEC manufacturing test.

M23: ATA/AV Lucent APLL1_TEST

- Reserved for APLL1 (100MHz and 200MHz) test.
- Inputs to the APLL1 macro can be controlled from the chip pins.
- Output of the APLL1 macro can be observed at the chip pin.

M24: ATA/AV Lucent APLL2_TEST

- Reserved for APLL2 (66.6MHz and 133MHz) test.
- Inputs to the APLL2 macro can be controlled from the chip pins.
- Outputs of the APLL2 macro can be observed at the chip pins.

M25: ATA/AV NEC APLL1_TEST

- Reserved for NEC APLL1 test.

M26: ATA/AV NEC APLL2_TEST

- Reserved for NEC APLL2 test.

5.4 PROGRAMMABLE IO PORT ASSIGNMENTS AND PULL-UP REQUIREMENTS

Table 5-2: ASIC Programmable Port Assignments: ATA

Pin Number	Pin Description	Assignment	Pull-Up Resister
104	MAD0/Port 1.0	MTR_ID	Y
105	MAD1/Port 1.1	HTEMP	Y
106	MAD2/Port 1.2	GMR_SELECT	Y
107	MAD3/Port 1.3	LEDON	Y
108	MAD4/Port 1.4	SMODE	N
109	MAD5/Port 1.5	DWENA	Y
110	MAD6/Port 1.6	SKCOMP	Y
111	MAD7/Port 1.7 Port 2.1 IN	RETRACT Internally Tied High	N
120	MAD15/Port 2.2	PWR_FLT_INT	Y
119	MAD14/Port 2.4	PARK_IDE	Y
5	HRESINT/Port 2.5	CABLE_SELECT_IDE	Y
114	MAD9/Port 2.6	DS_IDE	Y
115	MAD10/Port 2.7	CS_IDE	Y
116	MAD11/Port 3.5	VPCNTL	N
117	MAD12/Port 3.6	FLASH_CS	Y
118	MAD13/Port 3.7	SCOPETRIG	Y

Table 5-3: ASIC Programmable Port Assignments: AV

Pin Number	Pin Description	Assignment	Pull-Up Resister
25	HD0/Port 1.0	MTR_ID	Y
22	HD1/Port 1.1	HTEMP	Y
20	HD2/Port 1.2	GMR_SELECT	Y
43	DASP/Port 1.3	LEDON	Y
37	PDIAG/Port 1.4	SMODE	N
11	HD5/Port 1.5	DWENA	Y
9	HD6/Port 1.6	SKCOMP	Y
8	HD8/Port 1.7	RETRACT	N
16	HD11/Port 2.2	PWR_FLT_INT	Y
19	HD12/Port 2.4	NC (No Connect)	Y
7	HD7/Port 3.5	VPCNTL	N
10	HD9/Port 3.6	FLASH_CS	Y
13	HD10/Port 3.7	SCOPETRIG	Y

Volume 2 Section 7
INTERNAL/EXTERNAL TIMING SPECIFICATIONS and FLOW DIAGRAMS

7.1 MICROPROCESSOR INTERFACE TIMING

For information, see the NEC Microprocessor Interface Timing Specification.

7.2 BUFFER INTERFACE TIMING

This section provides detailed infromation of the electrical characterstics and the timing of the buffers.

7.2.1 Electrical Characteristics and Recommended AC Operating Conditions

The following diagrams show the behavior of buffer interface signals during read and write sessions to DRAM type buffers.

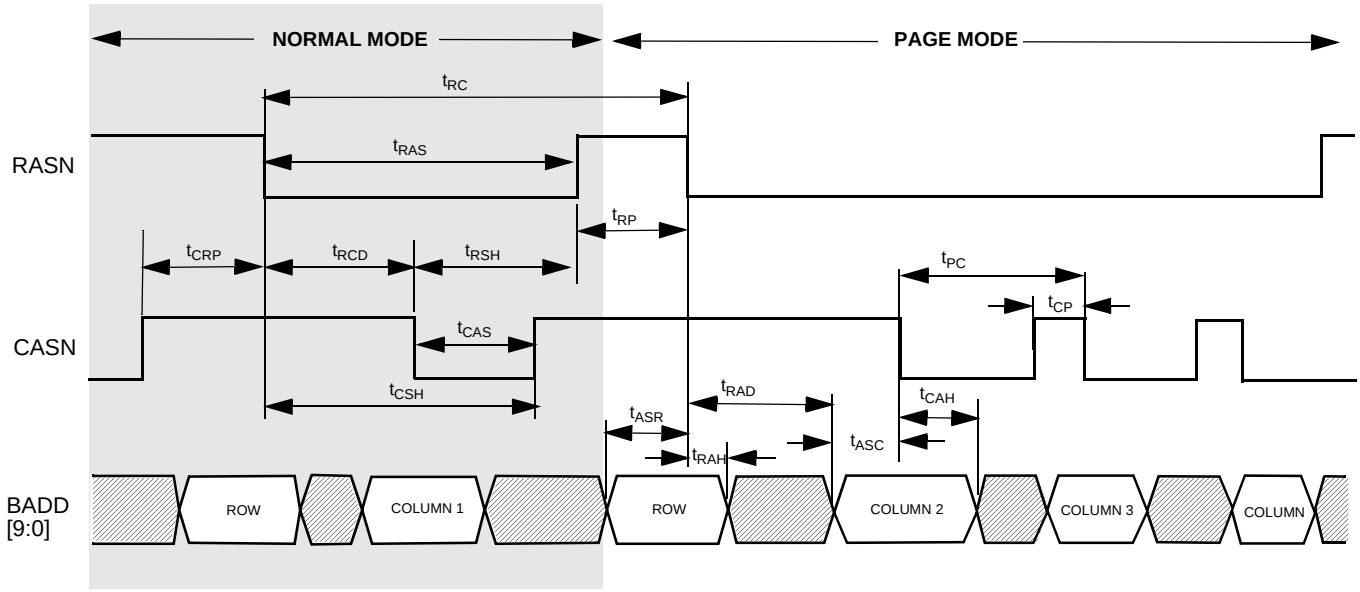


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Figure 7-1: DRAM Read Timing

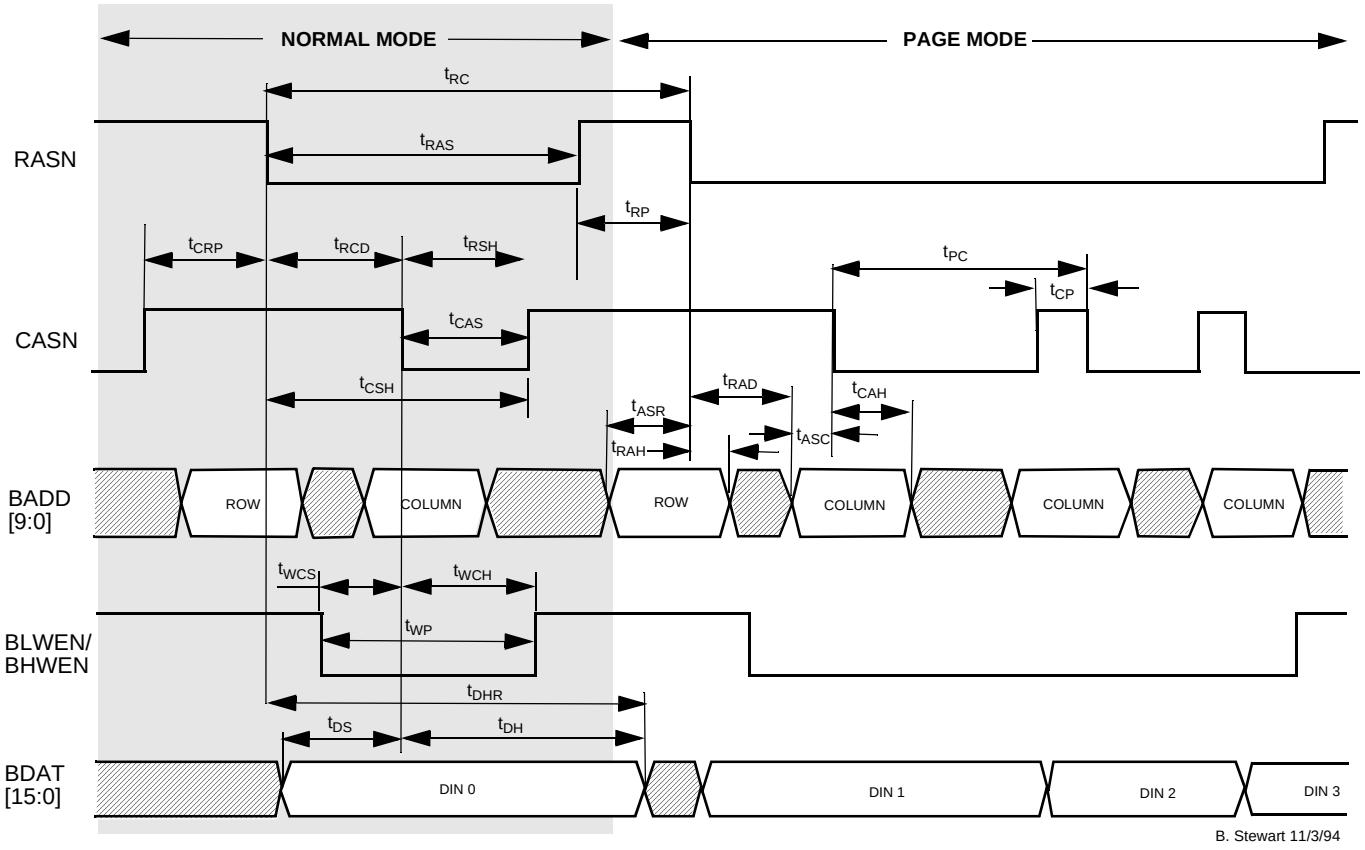

Figure 7-2: DRAM Write Cycle Timing

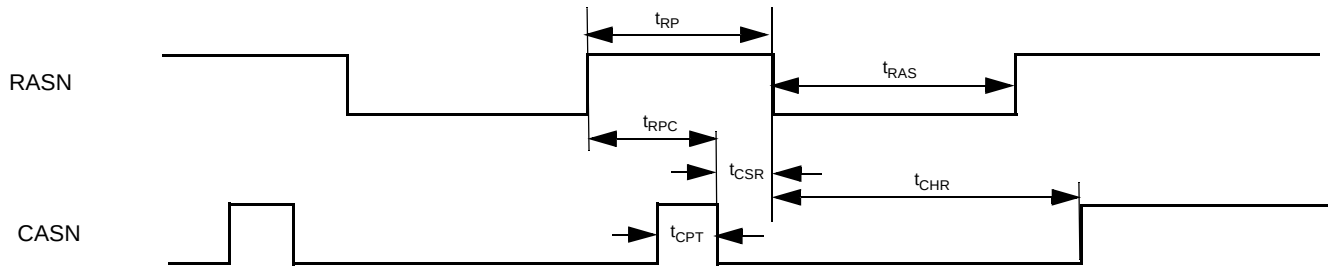

Figure 7-3: Refresh Timing

7.2.2 Buffer Delay Margins

Table 7-1 summarizes the delay margins between the ASIC design and the NEC DRAM specifications. as published in the 1995 NEC DRAM Data Book.

Table 7-1: 60 nSec. EDO DRAM Delay Margins

BUFFER AC PARAMETERS	Ivory DELAY VALUES				
	DESIGN		SPEC.	MARGIN	
	Min.	Max.		Min.	Max.
BUFFER READ CYCLE					
tRC (RAS cycle)	120	120	104	16	16
tRP (RAS pulse width)	45	45	40	5	5
tRAS (Width of RAS)	75	75	60	15	15
tCAS (Width of CAS)	11	19	10	1	9
tRCD (from neg edge RAS to neg edge CAS)	45	45	14	31	31
tRSH (from neg edge CAS to pos edge RAS)	30	30	10	20	20
tCSH (from neg edge RAS to pos edge CAS)	60	60	40	20	20
tCRP (from pos edge CAS to neg edge RAS)	60	60	5	55	55
tASR (addr setup time for neg edge RAS)	45	45	0	45	45
tRAH (addr hold time for neg edge RAS)	30	30	10	20	20
tASC (addr setup time for neg edge CAS)	15	15	0	15	15
tCAH (addr hold time for neg edge CAS)	11	19	10	1	9
tRAD (from neg edge RAS to valid col addr)	30	30	12	18	18
tRAL (from valid col addr to pos edge RAS)	45	45	30	15	15
tCP (CAS pulse width in page mode)	11	19	10	1	9
tPC (CAS cycle in page mode)	30	30	25	5	5
BUFFER WRITE CYCLE					
tRC (RAS cycle)	120	120	104	16	16
tRP (RAS pulse width)	45	45	40	5	5
tRAS (Width of RAS)	75	75	60	15	15
tCAS (Width of CAS)	11	19	10	1	9
tRCD (from neg edge RAS to neg edge CAS)	45	45	14	31	31
tRSH (from neg edge CAS to pos edge RAS)	30	30	10	20	20
tCSH (from neg edge RAS to pos edge CAS)	60	60	40	20	20
tCRP (from pos edge CAS to neg edge RAS)	60	60	5	55	55
tASR (addr setup time for neg edge RAS)	45	45	0	45	45
tRAH (addr hold time for neg edge RAS)	30	30	10	20	20
tASC (addr setup time for neg edge CAS)	15	15	0	15	15
tCAH (addr hold time for neg edge CAS)	11	19	10	1	19
tRAD (from neg edge RAS to valid col addr)	30	30	12	18	18
tRAL (from valid col addr to pos edge RAS)	45	45	30	15	15
tCP (CAS pulse width in page mode)	11	15	10	1	9
tPC (CAS cycle in page mode)	30	30	25	5	5
tDS (data setup time for neg edge CAS)	45	45	0	45	45
tDH (data hold time for neg edge CAS)	11	19	10	1	9
tWCS (from neg edge WEN to neg edge CAS)	45	45	0	45	45
tWCH (from neg edge CAS to pos edge WEN)	30	30	10	20	20

Table 7-1: 60 nSec. EDO DRAM Delay Margins (Continued)

BUFFER AC PARAMETERS	Ivory DELAY VALUES				
	DESIGN		SPEC.	MARGIN	
	Min.	Max.		Min.	Max.
tWP (width of WEN)	75	75	10	65	65
tCWL (from neg edge WEN to pos edge CAS)	45	45	10	35	35
tRWL (from neg edge WEN to pos edge RAS)	75	75	10	65	65
tWRC (from neg edge RAS to pos edge WEN)	75	75	10	65	65
BUFFER REFRESH CYCLE					
tRC (RAS cycle)	120	120	104	16	16
tRP (RAS pulse width)	75	75	60	15	15
tCSR (from neg edge CAS to neg edge RAS)	15	15	5	10	10
tCHR (from neg edge RAS to pos edge CAS)	60	60	10	70	70
tRPC (from pos edge RAS to neg edge CAS)	75	75	5	70	70
tCP (CAS pulse width in refresh cycle)	75	75	18	57	57

7.3.1.3 Buffer Read Cycles

Figure 7-4 shows the read cycles of the BFR block with an internal clock to register read data for the DRAM protocol. Additional internal delay is provided on the BDAT input path to ensure sufficient hold time to clock in the data. It is assumed that the DRAM OEN (output enable) pin is always active.

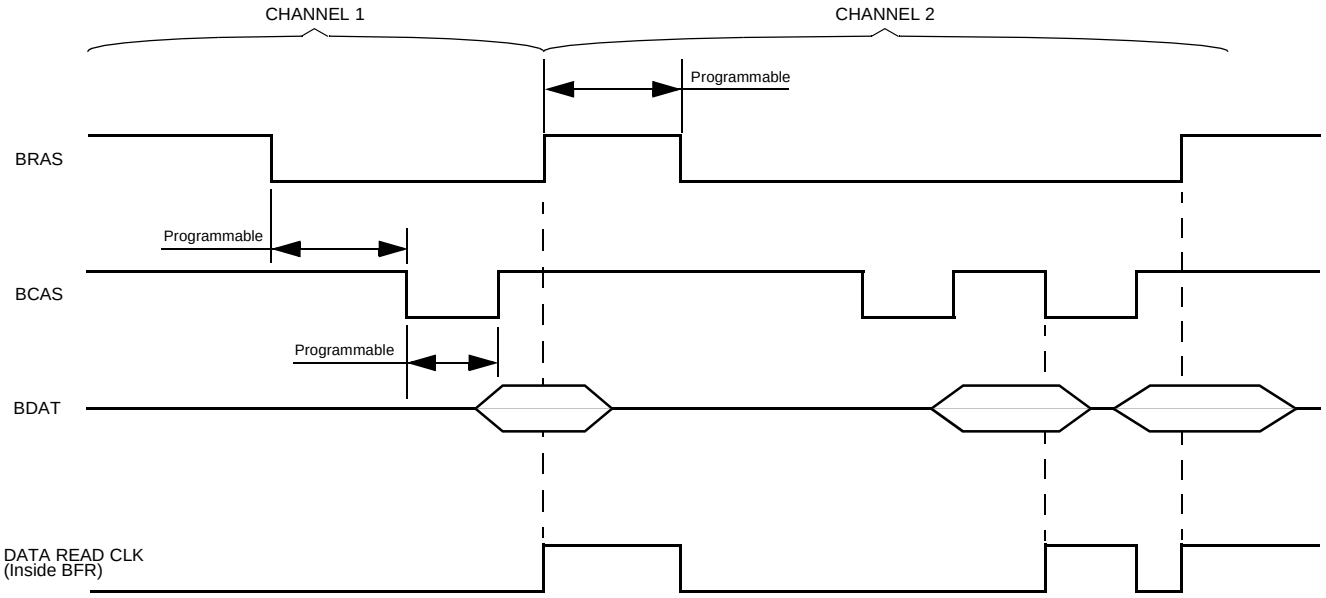

Figure 7-4: DRAM Reads For 2 Channels

7.4 1394 TIMING DIAGRAMS

7.4.1 TRANSACTION LAYER And ASIC INTERFACE TIMING

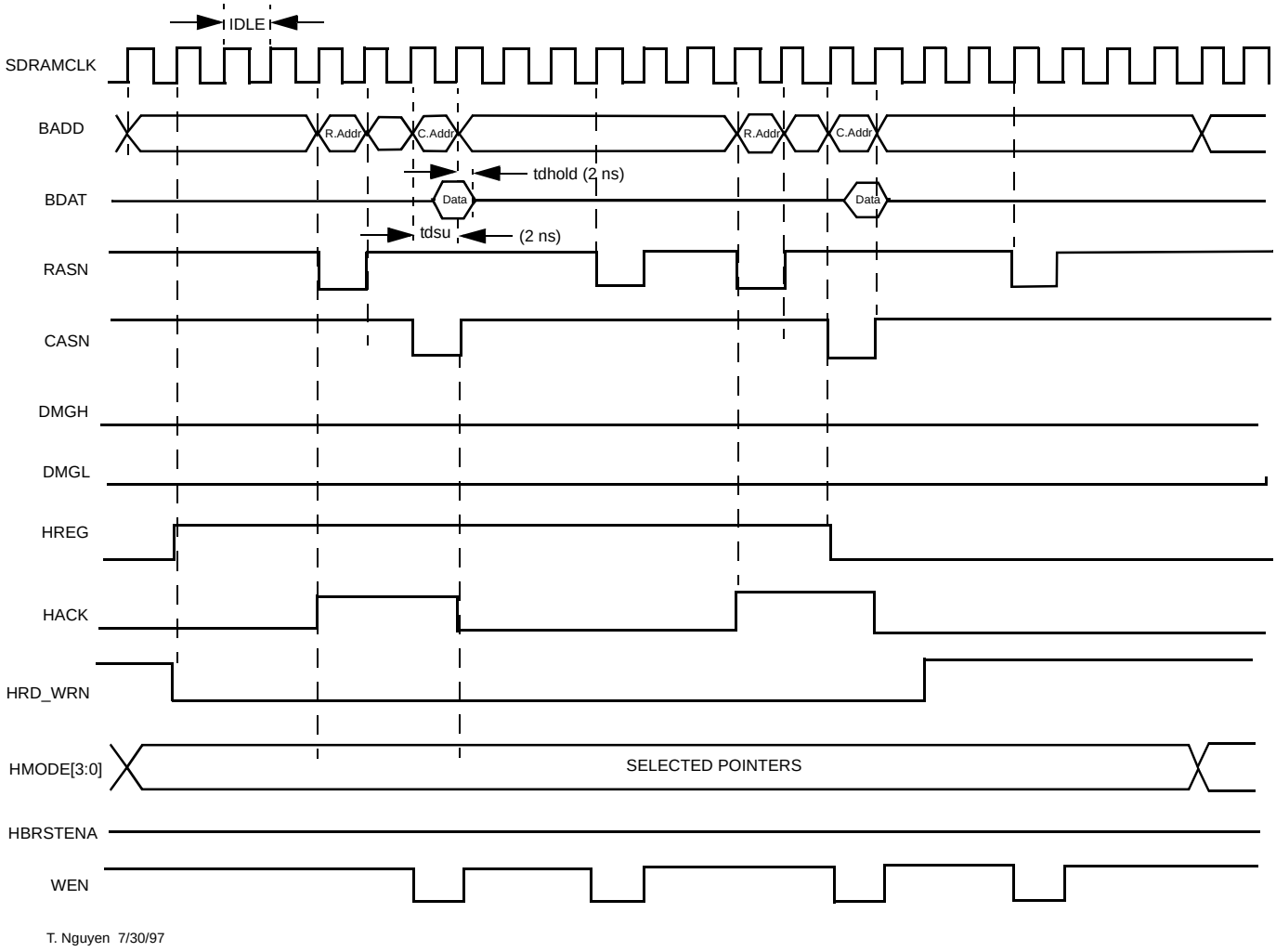

Figure 7-5: Transaction Layer Writes to SDRAM (HBRSTENA = 0)

Writes To SDRAM

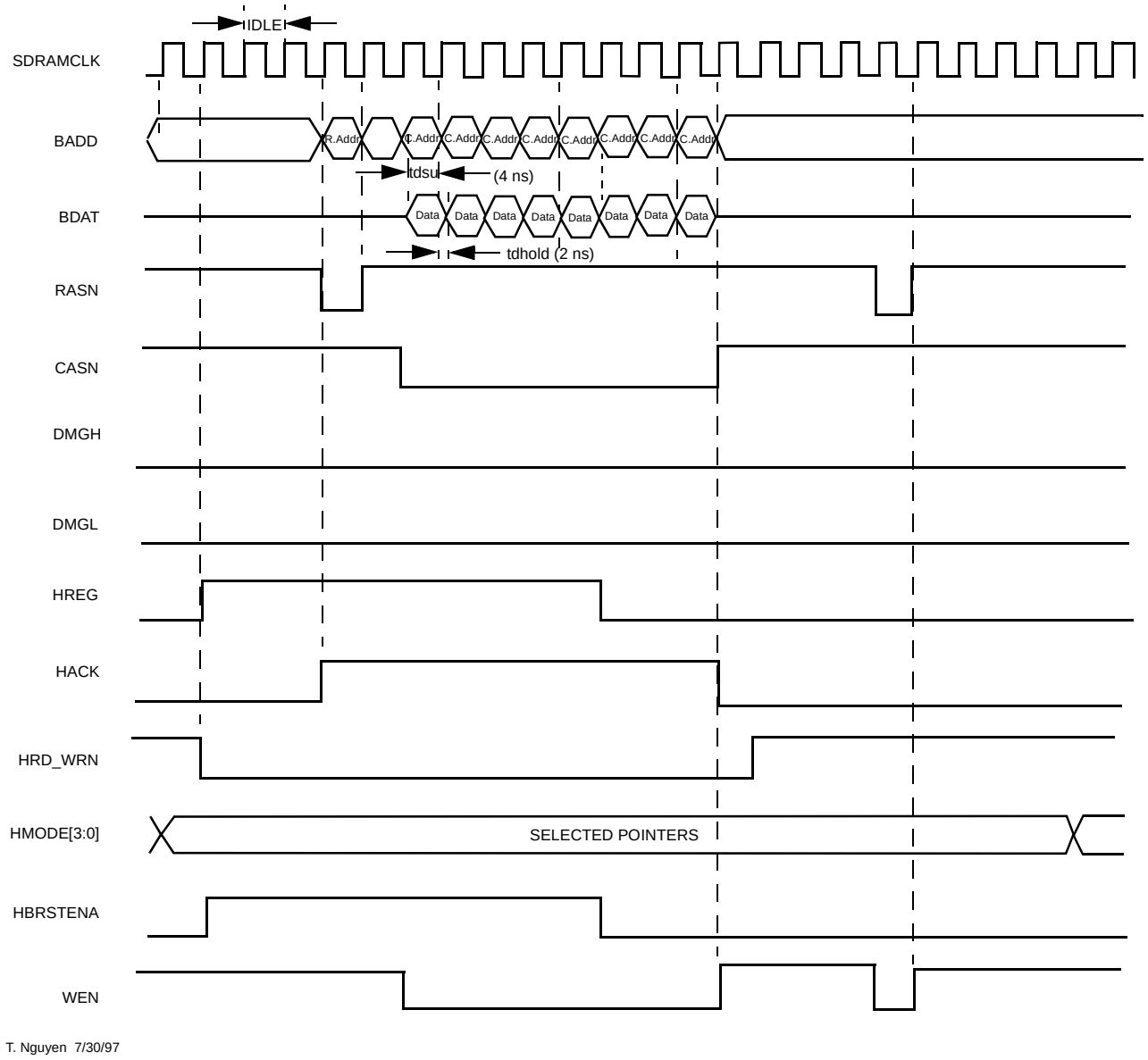

Figure 7-6: Transaction Layer Writes to SDRAM (HBRSTENA = 1)

Reads to SDRAM

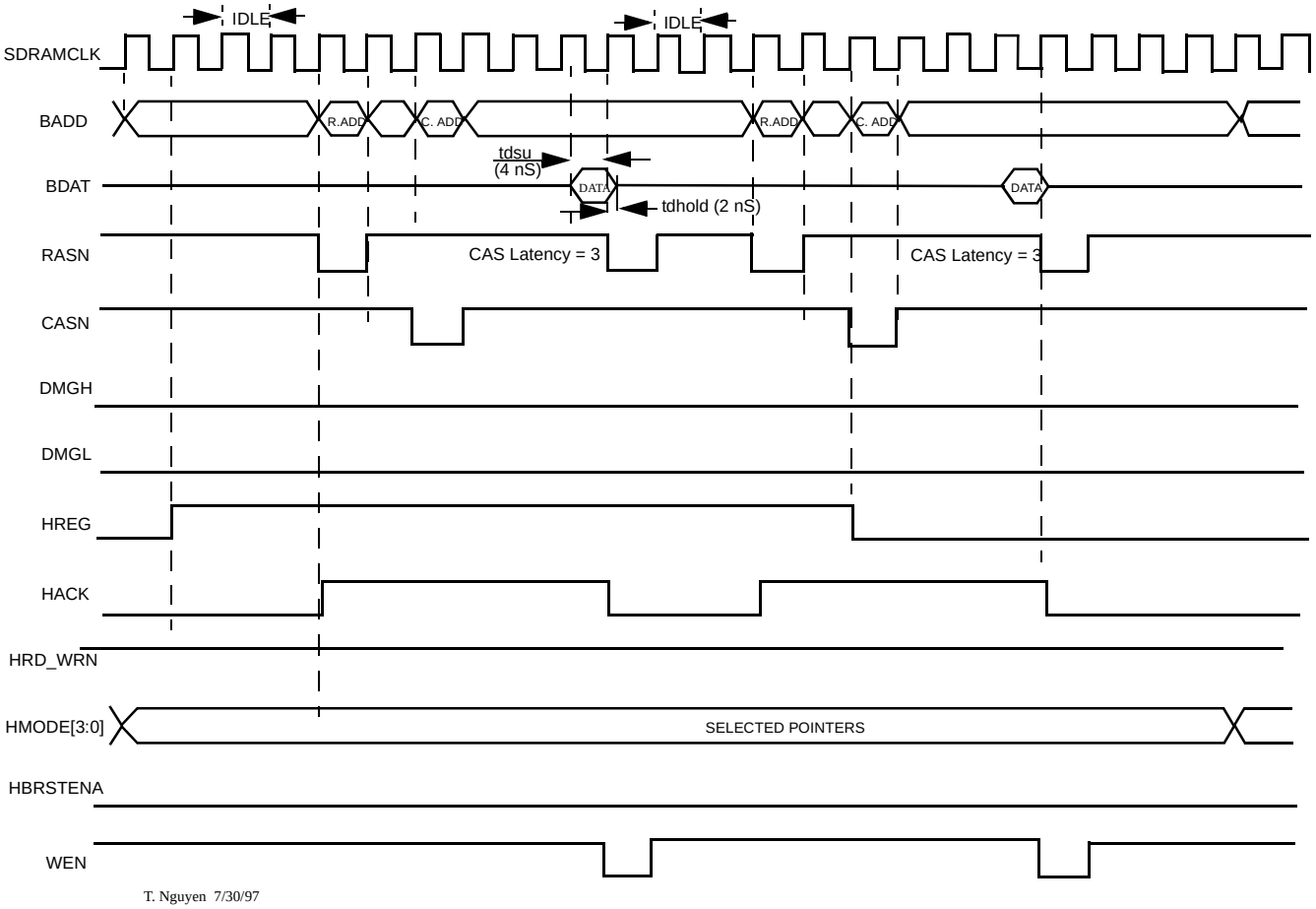

Figure 7-7: Transaction Layer Reads To SDRAM (HBRSTENA = 0)

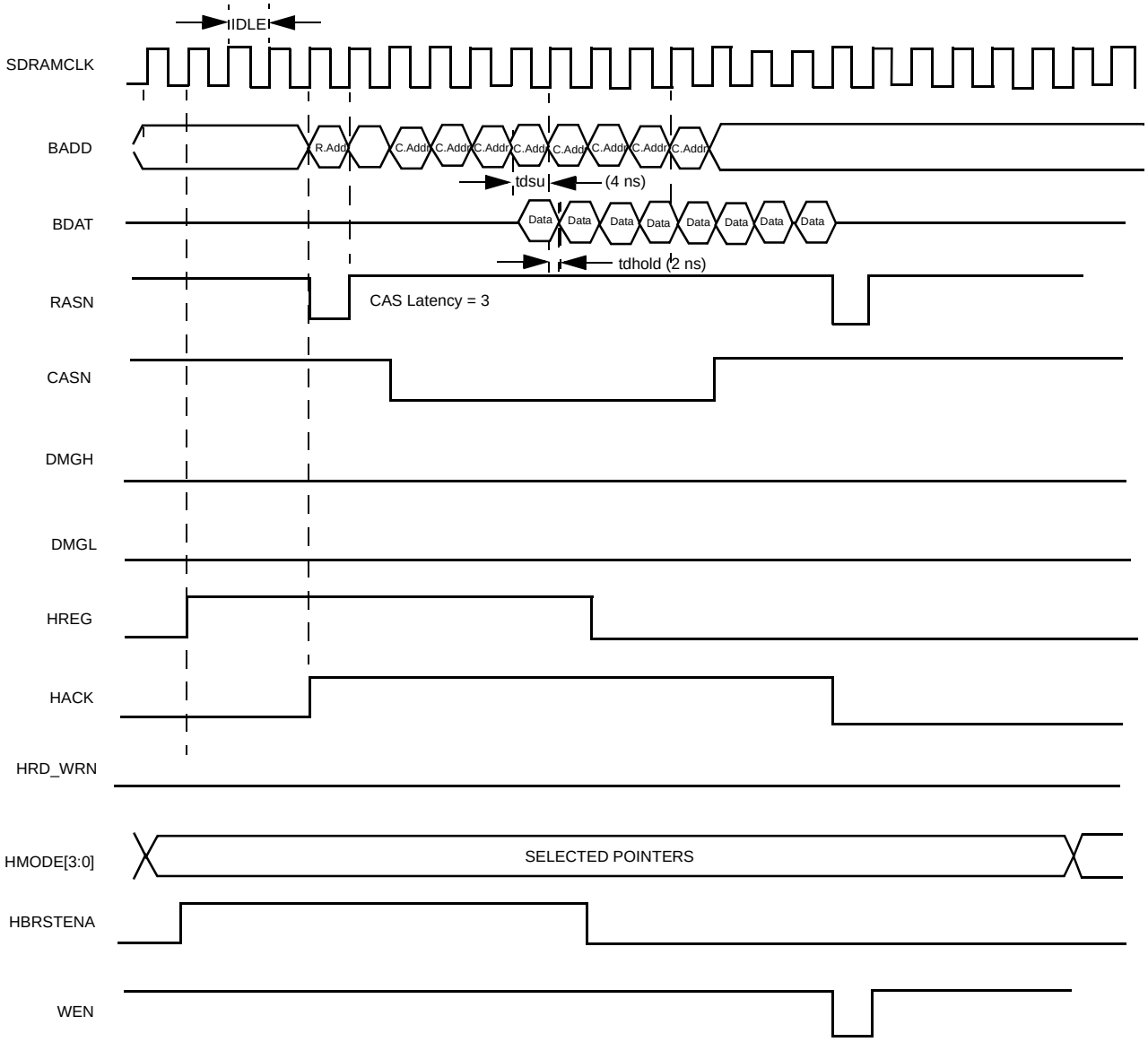

Figure 7-8: Transaction Layer Reads To SDRAM (HBRSTENA = 1)

Appendix A
AV Transfer Protocol

A.1 THEORY OF OPERATION

The ownership of SDRAM bus, including clock and control signals, are transferred between ASIC 1and ASIC 2. The hand shaking is executed through the signals hreq, hack, and cke. The following diagrams illustrate this operation:

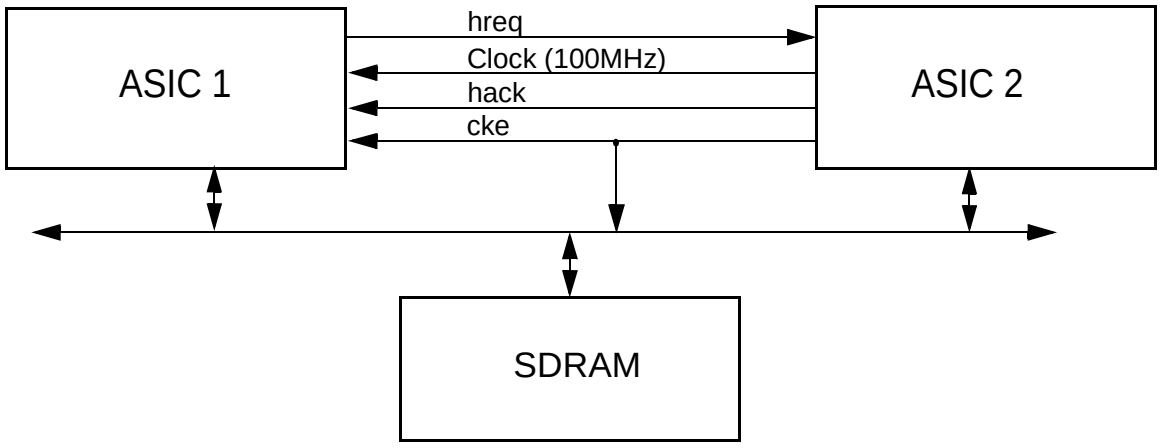

Figure A-1: SDRAM Bus

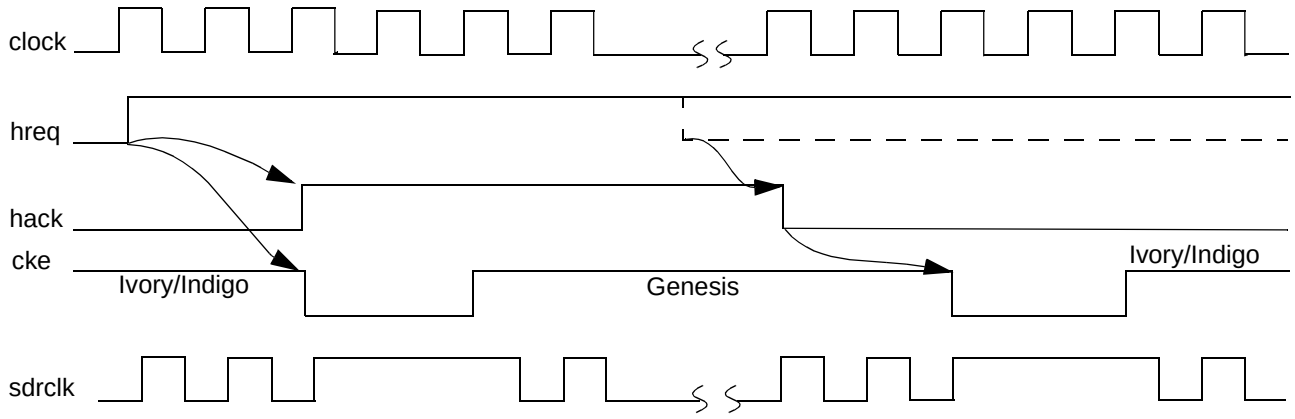

Figure A-2: Clock Timing

B

C

D

E

F

S

T

U

V

W

X

Z